



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/679,697	10/07/2003	Choong Un Lee	054358-5017	3567
9629	7590	09/08/2005	EXAMINER	
MORGAN LEWIS & BOCKIUS LLP 1111 PENNSYLVANIA AVENUE NW WASHINGTON, DC 20004			DUONG, THOI V	
			ART UNIT	PAPER NUMBER
			2871	
DATE MAILED: 09/08/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	10/679,697	LEE ET AL. 
	<b>Examiner</b>	<b>Art Unit</b>
Thoi V. Duong	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) Responsive to communication(s) filed on 22 June 2005.
- 2a) This action is **FINAL**.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-15 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 22 June 2005 is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) All    b) Some \* c) None of:
    1. Certified copies of the priority documents have been received.
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | Paper No(s)/Mail Date. _____  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>06/22/2005</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|   | 6) <input type="checkbox"/> Other: _____                                    |

## **DETAILED ACTION**

1. This office action is in response to the Amendment filed June 22, 2005.

Accordingly, claims 1, 6-9, 11, 12 were amended, and new claims 13-15 were added. Currently, claims 1-15 are pending in this application.

### ***Response to Arguments***

2. Applicant's arguments with respect to claims 1-12 have been considered but are moot in view of the new ground(s) of rejection.

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1, 2, 4, 6 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kodera et al. (Kodera, USPN 6,195,149 B1) in view of Hadoka et al. (Hadoka, JP 09-325328).

Re claim 1, as shown in Figs. 28-30, Kodera discloses a method of fabricating a liquid crystal display panel, comprising:

forming a plurality of upper liquid crystal display panel units 110a on a first mother substrate 101 and a plurality of liquid crystal display panel units 110a on a second mother substrate 104;

forming sealant patterns 106 on at least one of the mother substrates 101;

attaching the first and second mother substrates 101 and 104 to each other to bond the upper liquid crystal display units with associated ones of the lower liquid crystal display panel units to form at least first and second liquid crystal display panel units 110a;

forming at least first cutting lines 108 on each of the first and second mother substrates 101 and 104 (col. 1, lines 36-63), the first cutting lines 108 corresponding to a boundary of the first liquid crystal display panel unit 110a (upper portion in Fig. 29), wherein the first cutting lines 108 extend over the sealant pattern 106 (Fig. 31);

forming the second cutting lines 118 on each of the first and second mother substrates 101 and 104, the second cutting lines corresponding to a boundary of the boundary of the second liquid crystal display panel unit 110a (lower portion in Fig. 29); and

separating the first and second liquid display panel units into individual liquid crystal display panels 119 (Fig. 31).

However, Kodera does not disclose that the liquid crystal display panel units having at least two different sizes, wherein first liquid crystal display panel unit is larger than the second crystal display panel unit.

As shown in Fig. 1, Hakoda discloses a method of fabricating liquid crystal display panels comprising forming a first liquid display panel unit consisting of two individual liquid crystal panels 3 and a second liquid crystal display panel unit consisting of four individual liquid crystal panels 4 on a mother substrate 1, wherein the first liquid

crystal display panel unit is larger than the second crystal display panel unit (Abstract and Detail Description, paragraphs 7-9).

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of fabricating liquid crystal display panels of Kodera with the teaching of Hakoda by forming liquid crystal display panel units having at least two different sizes on mother substrates so as to reduce production cost (Abstract).

Re claim 2, as shown in Figs. 28 and 30, Kodera discloses that the first and second mother substrates 101 and 104 comprise a plurality of dummy glass substrates including main dummy glass substrates (long and narrow portions bordered by the surface cuts 108 in Fig. 28) and secondary dummy glass substrates (long and narrow portions bordered by the surface cuts 118 in Fig. 30).

Re claim 4, Kodera discloses that the sealant patterns 106(106a) are formed on non-display regions of the liquid crystal display panels 119.

Re claim 6, as shown in Fig. 28, Kodera discloses that sizes of the upper liquid crystal display panel units on the first mother substrate 101 and the lower liquid crystal display panel units on the second mother substrate 104 facing correspondingly at into each other are substantially the same.

Re claim 13, the method of Kodera further comprises injecting liquid crystals into the separated liquid crystal panel units 110a (col. 1, line 54 through col. 2, line 3).

5. Claims 5, 8, 9, 11, 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kodera et al. (Kodera, USPN 6,195,149 B1) in view of Hadoka et al. (Hadoka, JP 09-325328) and Shiraishi (USPN 6,864,947 B2).

As shown in Figs. 28-30, Kodera discloses a method of fabricating a liquid crystal display panel, comprising:

forming a plurality of upper liquid crystal display panel units 110a on a first mother substrate 101 and a plurality of liquid crystal display panel units 110a on a second mother substrate 104;

forming sealant patterns 106 on at least one of the mother substrates 101;

attaching the first and second mother substrates 101 and 104 to each other to bond the upper liquid crystal display units with associated ones of the lower liquid crystal display panel units to form at least first and second liquid crystal display panel units 110a;

forming at least first cutting lines 108 and second cutting lines 118 on each of the first and second mother substrates 101 and 104; and

separating the first and second liquid display panel units 110a from the attached mother substrates 101 and 104 (Fig. 29), wherein the separated mother substrates 101 and 104 include main dummy glass substrates and secondary dummy glass substrates divided by the first and second cutting lines 108 and 118 respectively (long-and-narrow portions bordered by the surface cuts 108 and 118 on the mother substrates 101 and 104).

Re claim 9, the method of Kodera further comprises injecting liquid crystals into the separated liquid crystal panel units 110a (col. 1, line 54 through col. 2, line 3).

Re claim 11, as shown in Fig. 28, Kodera discloses that sizes of the upper liquid crystal display panel units on the first mother substrate 101 and the lower liquid crystal display panel units on the second mother substrate 104 facing correspondingly at into each other are substantially the same.

However, Kodera does not disclose that the liquid crystal display panel units having at least two different sizes, and at least one of the sealant patterns located underneath the first cutting lines between the main dummy glass substrates and the second dummy glass substrates.

At first, as shown in Fig. 1, Hakoda discloses a method of fabricating liquid crystal display panels comprising forming a first liquid display panel unit consisting of two individual liquid crystal panels 3 and a second liquid crystal display panel unit consisting of four individual liquid crystal panels 4 on a mother substrate 1, wherein the first liquid crystal display panel unit is larger than the second crystal display panel unit (Abstract and Detail Description, paragraphs 7-9).

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of fabricating liquid crystal display panels of Kodera with the teaching of Hakoda by forming liquid crystal display panel units having at least two different sizes on mother substrates so as to reduce production cost (Abstract).

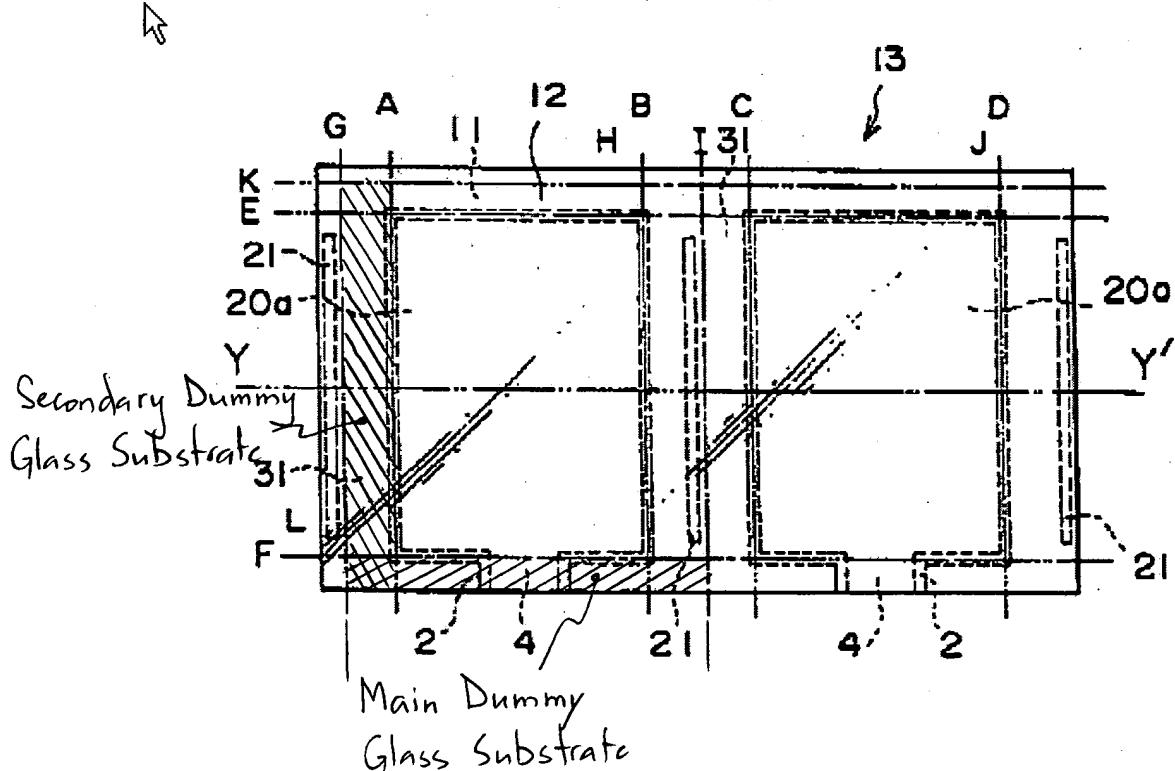
Art Unit: 2871

Further, as shown in Figs. 8A and 8B, Shiraishi discloses a method of fabricating a liquid crystal display panel, comprising:

separating liquid crystal display panels 20a from the attached mother substrates, wherein the attached mother substrates include main dummy glass substrates and secondary dummy glass substrates divided by the first and second cutting lines A, F, and G, and the sealant pattern 2 is located underneath the first cutting line F between the main dummy glass substrates and the secondary dummy glass substrates (underneath the terminal portion 31) (see Fig. 8A below).

Re claim 5, the sealant pattern 2 is positioned on both the main dummy glass substrates and the second dummy glass substrates as shown below in Fig. 8A.

**FIG. 8A**



Art Unit: 2871

Re claims 14 and 15, since the sealant pattern 2 is adhesive under the first cutting lines, and the sealant pattern 2 is formed along the main dummy glass substrates and secondary dummy glass substrates, it is obvious that the sealant pattern 2 binds the main dummy glass substrates and secondary dummy glass substrates together during the separating step.

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the method of fabricating the liquid crystal display panels of Kodera] with the teaching of Shiraishi by forming at least one of the sealant patterns located underneath the first cutting lines between the main dummy glass substrates and the second dummy glass substrates so as to obtain an appropriate cutting surface without receiving an influence of the bias of the stress due to the sealing pattern (col. 11, lines 3-10).

6. Claims 3 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kodera et al. (Kodera, USPN 6,195,149 B1) in view of Hadoka et al. (Hadoka, JP 09-325328) as applied to claims 1, 2, 4, 6 and 13 above and further in view of Nakahara et al. (Nakahara, USPN 6,239,855 B1).

As shown in Fig.11, Kodera discloses the second substrates 4 having a plurality of thin film transistors and a plurality of pixel electrodes 7, and the first substrates 1 having a common electrode 2 (col. 3, lines 38-52 and col. 8, lines 29-64).

However, Kodera does not disclose a method for forming a plurality of color filters on the first substrates and the secondary dummy glass substrates having a width of less than about 3 mm.

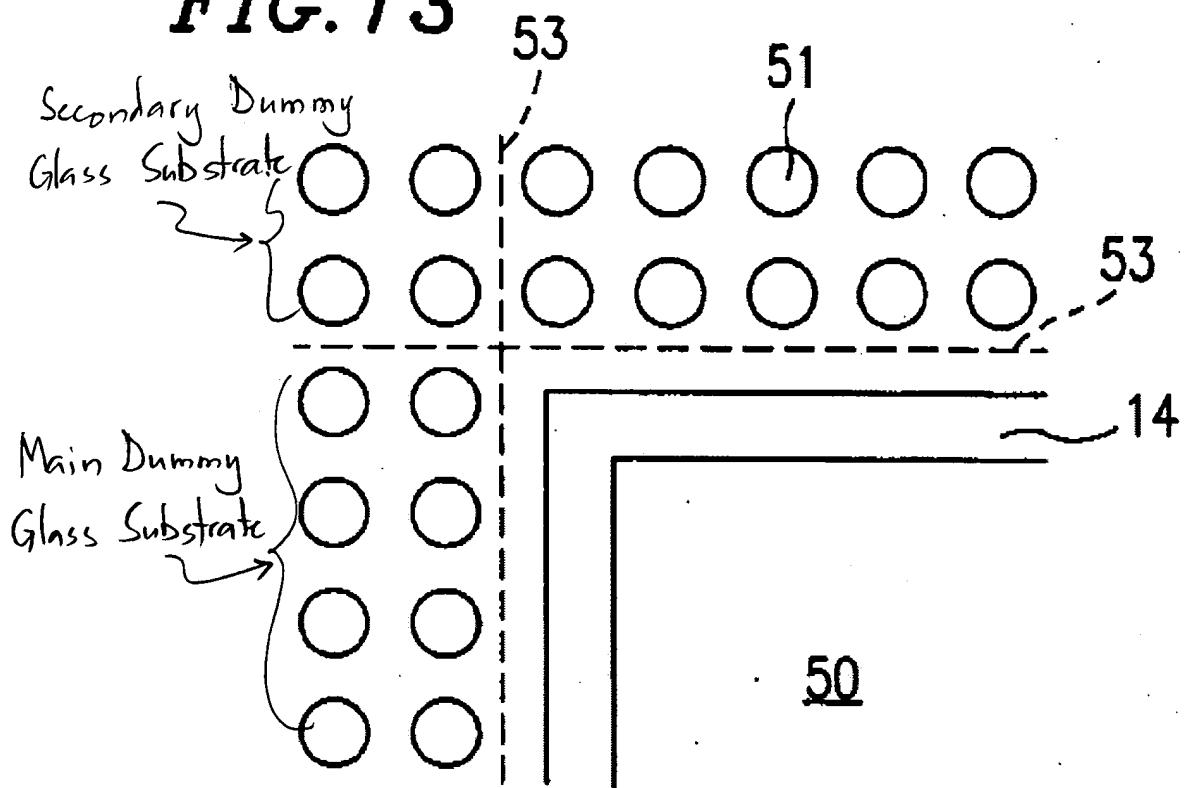
As shown in Fig. 1, Nakahara discloses that a color filter can be formed on at least one of the substrates (col. 9, lines 4-5).

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Kodera by

Re claim 3, Kodera discloses a method of fabricating a liquid crystal display panel that is basically the same as that recited in claim 3 except for

As shown in Figs. 2 and 13, Nakahara discloses a method of fabricating a liquid crystal display panel 50 comprising forming a plurality of dummy glass substrates 22 (seal formation area) including main dummy glass substrates (vertical portion) and secondary glass substrates (horizontal portion) around sealant patterns 14 (see Fig. 13 below), wherein the dummy glass substrates comprises sealant particles 51 having a diameter of 0.2 mm and an interval of 0.6 mm between adjacent sealant particles (col. 12, lines 30-42). Accordingly, the width of the dummy glass substrates in Fig. 13 is less than 3 mm. Also, the sealant patterns 14 are positioned on both the main and secondary dummy glass substrates.

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the method of fabricating a liquid crystal display panel of Kodera with the teaching of Nakahara by forming a plurality of color filters on the first substrates for obtaining a color display and forming the dummy glass substrates around the liquid crystal panel to provide a uniform cell gap in the vicinity of injection sealant patterns (col. 7, lines 5-11).

**FIG. 13**

7. Claims 10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kodera et al. (Kodera, USPN 6,195,149 B1) in view of Hadoka et al. (Hadoka, JP 09-325328) and Shiraishi (USPN 6,864,947 B2).as applied to claims 5, 8, 9, 11, 14 and 15 above, and further in view of in view of Nakahara et al. (Nakahara, USPN 6,239,855 B1).

As shown in Fig.11, Kodera discloses the second substrates 4 having a plurality of thin film transistors and a plurality of pixel electrodes 7, and the first substrates 1 having a common electrode 2 (col. 3, lines 38-52 and col. 8, lines 29-64).

However, Kodera does not disclose a method for forming a plurality of color filters on the first substrates and the secondary dummy glass substrates having a width of less than about 3 mm.

As shown in Fig. 1, Nakahara discloses that a color filter can be formed on at least one of the substrates (col. 9, lines 4-5).

Further, as shown in Figs. 2 and 13, Nakahara discloses a method of fabricating a liquid crystal display panel 50 comprising forming a plurality of dummy glass substrates 22 (seal formation area) including main dummy glass substrates (vertical portion) and secondary glass substrates (horizontal portion) around sealant patterns 14 (see Fig. 13 above), wherein the dummy glass substrates comprises sealant particles 51 having a diameter of 0.2 mm and an interval of 0.6 mm between adjacent sealant particles (col. 12, lines 30-42). Accordingly, the width of the dummy area in Fig. 13 is less than 3 mm.

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the method of fabricating a liquid crystal display panel of Kodera with the teaching of Nakahara by forming a plurality of color filters on the first substrates for obtaining a color display and forming the dummy glass substrates having a width of less than about 3 mm to provide a uniform cell gap in the vicinity of injection sealant patterns (col. 7, lines 5-11).

### ***Conclusion***

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

Art Unit: 2871

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thoi V. Duong whose telephone number is (571) 272-2292. The examiner can normally be reached on Monday-Friday from 8:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim, can be reached at (571) 272-2293.

Thoi Duong



08/29/2005

  
DUNG T. NGUYEN  
PRIMARY EXAMINER

REPLACEMENT SHEET



Approved  
End 08/29/05

Fig. 2

